In the Claims:

1. (Currently Amended) A method of incorporating a first dielectric material having a first dielectric constant into a semiconductor device, said semiconductor device being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said semiconductor device at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant, and a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop, an etch stop layer, and disposed adjacent at least one conductive line of said semiconductor device;

removing at least a portion of said second dielectric material down to said etch stop layer subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The method of claim 1 wherein said at least one conductive line includes a contact barrier layer, and the thermal processing step is an anneal step of said contact barrier layer.

5. (Canceled)

6. (Canceled)

7. (Previously Presented) The method of claim 1 further comprising:

planarizing said first dielectric material to a top surface of said conductive line; and

depositing a further layer of said first dielectric material atop said layer of said planarized first dielectric material and atop said conductive line.

8. (Previously Presented) The method of claim 1 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and said method further includes planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

9. (Currently Amended) A method of incorporating a first dielectric material having a first dielectric constant into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant and ~~that has~~ a maximum withstand temperature greater than the temperature of the thermal processing step, said fabricating step comprising:

depositing a first layer of said second dielectric material atop a surface of a semiconductor substrate,

planarizing said first layer of said second dielectric material to a top surface of another conductive line disposed atop said semiconductor substrate,

depositing another layer of said second dielectric material atop said first layer of said second dielectric material and atop said another conductive line,

patterning and etching said another layer of said second dielectric material to form at least one opening therein, and

filling said opening with at least one conducting material to form said at least one conductive line;

removing at least a portion of said second dielectric material subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

10. (Canceled)

11. (Canceled)

12. (Previously Presented) The method of claim 9 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material.

13. (Previously Presented) The method of claim 9 wherein an etch stop layer is disposed beneath said second dielectric material; and wherein said step of removing at least a portion of said second dielectric material includes etching down to said etch stop layer.

14. (Previously Presented) The method of claim 9 wherein said step of removing at least a portion of said second dielectric material includes a timed etching step.

15. (Previously Presented) The method of claim 9 further comprising:

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

16. (Previously Presented) The method of claim 9 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

17.-52. (Canceled)

53. (Currently Amended) A method of incorporating first dielectric material <u>having a first dielectric constant</u> into an insulator structure that is adjacent to at least one conductive line of a

semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant, and ~~that has~~ a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop an etch stop layer;

removing at least a portion of said second dielectric material down to said etch stop layer subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

54. (Canceled)

55. (Previously Presented) The method of claim 53 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material.

56. (Previously Presented) The method of claim 53 further comprising:

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

57. (Previously Presented) The method of claim 53 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

58. (Currently Amended) A method of incorporating first dielectric material having a first dielectric constant into an insulator structure that is adjacent at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant, and ~~that has~~ a maximum withstand temperature greater than the temperature of the thermal processing step, said fabricating step comprising depositing a contact barrier layer prior to forming said at least one conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material;

removing at least a portion of said second dielectric material subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said dielectric material.

59. (Currently Amended) A method of incorporating first dielectric material having a first dielectric constant into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant, and ~~that has~~ a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said second dielectric material subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material;

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

60. (Currently Amended) A method of incorporating a first dielectric material having a first dielectric constant into a semiconductor device, said semiconductor device being fabricated by a

process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said semiconductor device at least through the thermal processing step using a second dielectric material having a second dielectric constant greater than said first dielectric constant, and a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop an etch stop layer;

removing at least a portion of second dielectric material down to said etch stop layer subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

61. (Canceled)

62. (Previously Presented) The method of claim 53 wherein said at least one conductive line includes a contact barrier layer, and the thermal processing step is an anneal step of said contact barrier layer.

63. (Currently Amended) A method of incorporating a first dielectric material having a first dielectric constant into a layer of an electronic structure that includes ~~to~~ at least one conductive line of a semiconductor device, said layer of electronic structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said layer of electronic structure and said at least one conductive line at least through the thermal processing step, said layer comprising having a second dielectric constant greater than said first dielectric constant, and a second dielectric material lying adjacent said at least one conductive line and said second dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said second dielectric material from said layer subsequent to said thermal processing step; and then

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

64. (Canceled)

65. (Previously Presented) The method of claim 63 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material.

66. (Previously Presented) The method of claim 63 wherein said step of removing at least a portion of said second dielectric material includes a timed etching step.

67. (Previously Presented) The method of claim 63 further comprising:

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

68. (Previously Presented) The method of claim 63 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.